

S/N 09/866,938

#411102
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wendell P. Noble et al.

Serial No.: 09/866,938

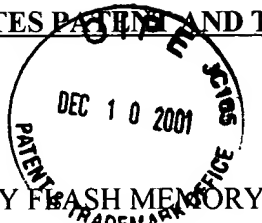
Filed: May 29, 2001

Title: ULTRA HIGH DENSITY FLASH MEMORY

Examiner:

Group Art Unit: 2813

Docket: 303.330US3



SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialled by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Under 37 C.F.R. §1.97(b)(3), it is believed that no fee or certificate is required with this Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

WENDELL P. NOBLE ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date

11/28/2001

By

Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 28 day of November, 2001.

Gina M. Uphus

Name

Signature

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DEC 13 2001
TC 2800 MAIL ROOM



Sheet 1 of 1

Form 1449*

Atty. Docket No.: 303.330US3

Serial No. 09/866,938

INFORMATION DISCLOSURE STATEMENT
BY APPLICANT
(Use several sheets if necessary)

Applicant: Wendell P. Noble et al.

Filing Date: May 29, 2001

Group: 2813

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
						If Appropriate
	4,252,579	02/24/1981	Ho, I.T., et al.	148	174	05/07/79
	4,929,988	05/29/1990	Yoshikawa, K.	357	23.5	08/23/88
	5,874,760	02/23/1999	Burns, Jr., S.M., et al.	257	315	01/22/97
	5,943,267	08/24/1999	Sekariapuram, S., et al.	365	185.28	06/12/98
	6,172,391	01/09/2001	Goebel, B.	257	305	08/27/98
	6,221,788	04/24/2001	Kobayashi, H., et al.	438	762	12/18/98
	6,255,708	07/03/2001	Sudharsanan, R., et al.	257	428	10/10/97

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation
						Yes No
	2000-164883	06/16/2000	Japan	H01L	29/786	

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial

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Examiner

Date Considered

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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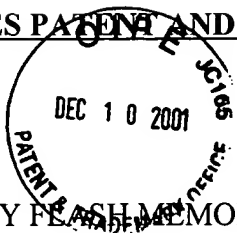
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COMMUNICATION CONCERNING CO-PENDING APPLICATION(S)

Commissioner for Patents
Washington, D.C. 20231

Applicant would like to bring to the Examiner's attention the following related co-pending application(s) in the above-identified patent application:

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<u>Serial No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/527,981	03/17/2000	00303.322US2	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES
09/571,352	05/16/2000	00303.322US3	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES
09/510,095	02/22/2000	00303.323US2	SEMICONDUCTOR-ON-INSULATOR MEMORY CELL WITH BURIED WORD AND BODY LINES
09/139,164	08/24/1998	00303.328US2	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES
09/596,266	06/16/2000	00303.328US3	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES
09/651,199	08/30/2000	00303.328US4	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES
09/789,274	02/20/2001	00303.329US4	MEMORY CELL WITH VERTICAL TRANSISTOR AND BURIED WORD AND BODY LINES

COMMUNICATION CONCERNING CO-PENDING APPLICATIONS

Serial Number: 09/866,938

Filing Date: May 29, 2001

Title: ULTRA HIGH DENSITY FLASH MEMORY

Page 2

Dkt: 303.330US3

09/551,027	04/17/2000	00303.379US2	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
08/944,890	10/06/1997	00303.380US1	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/730,245	12/05/2000	00303.380US3	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/467,992	12/20/1999	00303.389US2	CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED SEMICONDUCTOR SURFACES
09/742,568	12/20/2000	00303.393US3	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/669,281	09/26/2000	00303.405US3	PROGRAMMABLE MEMORY ADDRESS DECODE ARRAYS WITH VERTICAL TRANSISTOR
09/520,494	03/08/2000	00303.406US2	FIELD PROGRAMMABLE LOGIC ARRAYS WITH VERTICAL TRANSISTORS
09/756,089	01/08/2001	00303.407US2	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS
09/756,099	01/08/2001	00303.407US3	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS
09/650,600	08/30/2000	00303.408US2	MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS
09/879,592	06/12/2001	00303.412US2	VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS

COMMUNICATION CONCERNING CO-PENDING APPLICATIONS

Serial Number: 09/866,938

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Page 3

Dkt: 303.330US3

MEMORY AND METHOD FOR
FORMING THE SAME

09/879,602 06/12/2001 00303.412US3

VERTICAL GAIN CELL AND ARRAY
FOR A DYNAMIC RANDOM ACCESS
MEMORY AND METHOD FOR
FORMING THE SAME

09/498,433 02/04/2000 00303.464US2

CIRCUITS AND METHODS FOR A
MEMORY CELL WITH A TRENCH
PLATE TRENCH CAPACITOR AND A
VERTICAL BIPOLAR READ DEVICE

Respectfully submitted,

WENDELL P. NOBLE ET AL.

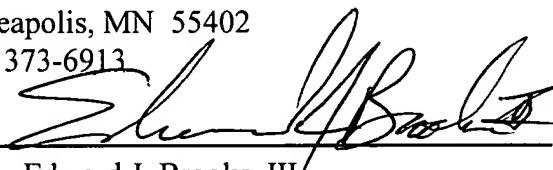
By Applicant's Representatives,

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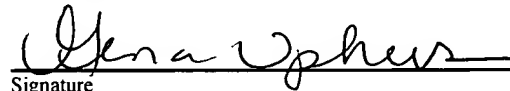
Edward J. Brooks, III

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Gina M Uphus

Name



Signature